Amendments To The Specification

Please replace paragraph [0007] with the following amended paragraph:

[0007] If an NMOS or Ndevice is to be formed, enhanced electron mobility or enhanced performance may be accomplished by locating the NMOS channel region in a silicon layer 4 under biaxial tensile strain. This is schematically shown in ~~Fig~~ Fig. 2. The silicon layer 4 may be epitaxially grown over the underlying silicon-germanium layer 2a. The silicon layer 4 may have a thickness between about 20 to 100 Angstroms. Again to avoid consumption of the material used to accommodate the device channel region during gate insulator formation, a silicon capping layer 3, is formed over the silicon layer 4. If desired, the process herein may also be applied to an NMOS device in which a silicon layer, under biaxial tensile strain, overlays a silicon-germanium layer.

Please replace paragraph [0008] with the following amended paragraph:

[0008] In FIG. 3, a gate insulator layer 24, comprised of silicon dioxide may be thermally grown to a thickness between about 8 to 50 Angstroms, for example, over the silicon capping layer 3. A conductive layer such as a doped polysilicon layer 5, may be deposited via low pressure chemical vapor deposition (LPCVD) to a thickness between about 600 to 2000 Angstroms, for example. The polysilicon layer 5 may be doped in situ during deposition via the addition of arsine or phosphine to a silane ambient, or the polysilicon layer 5 may be deposited intrinsically then doped via implantation of arsenic or phosphorous ions. If lower line resistance is desired, a composite layer (not shown) comprised of an underlying doped ~~polysifcon~~

polysilicon layer and an overlying metal silicide layer may be employed. The metal silicide layer can be a titanium silicide or tungsten silicide layer, for example, or other suitable materials. A photoresist may be used to pattern etch and define conductive gate structure from the polysilicon layer 5. An anisotropic reactive ion etching (RIE) procedure may be used using chlorine or flourine-based gas as a selective etchant for the polysilicon, or for the composite layer. Removal of the photoresist may be accomplished using known or later developed plasma oxygen ashing and wet clean procedures. A buffered hydrofluoric acid component of the wet clean procedure may remove a portion of the gate insulator layer 24 not covered by the polysilicon layer 5.

Please replace paragraph [0011] with the following amended paragraph:

[0011] Referring to FIG. 5, partial removal of silicon-germanium layer 2a, is accomplished via a selective anisotropic RIE procedure, using Cl_2, or SF_6, or a flourine-based gas as an etchant, for example. The remaining silicon germanium portion 2b may have a reduced thickness between about 20 to 200 Angstroms. The thinner silicon-germanium layer 2b may result in less germanium segregation at the surfaces of a metal silicide region during a silicidation procedure, when compared to counterpart metal silicide regions formed on thicker silicon-germanium layers. Total removal of exposed portions of silicon-germanium, shown schematically in Fig. 6 may be accomplished via a more prolonged selective anisotropic RIE procedure. In other words, by varying the process time of the etching process, the silicon germanium layer 2a may be partially or totally removed depending on the desired result. In both examples the selectivity of the RIE procedure features the non-etching of insulator spacers 6, however the conductive gate structure 5 may be thinned during the anisotropic RIE procedure used to partially or totally remove silicon-germanium from the top surface of source/drain regions 7.